Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 3. (Cancelled)

4. (Currently Amended) ~~The master slice semiconductor integrated circuit according to claim 1,~~ A master slice semiconductor integrated circuit, comprising:

at least two wiring layers for wiring; and

a plurality of clock buffers connected by clock wirings in a form of a clock tree having at least two cascaded stages to distribute clock signals to a plurality of sequential circuits;

wherein each of said clock wirings among said plurality of clock buffers comprises a wiring layer switching portion which switches a clock wiring from a lower wiring layer of said at least two wiring layers to an upper wiring layer of said at least two wiring layers and then switches said clock wiring from said upper wiring layer to said lower wiring layer;

wherein said wiring layer switching portion comprises:

an output wiring which is formed of said lower wiring layer and connects one end thereof to ~~the~~ a clock output of ~~the~~ a clock buffer of a former stage;

an output side via wiring which connects one end thereof to the other end of said output wiring and connects the other end thereof to said upper wiring layer;

an input wiring which is formed of said lower wiring layer and connects one end thereof to ~~the~~ a clock input of ~~the~~ a clock buffer of a later stage; and

an input side via wiring which connects one end thereof to the other end of said input wiring and connects the other end thereof to said upper wiring layer; and

wherein said upper wiring layer is a wiring layer for customized wirings, and said lower wiring layer is a wiring layer for fixed wirings.

5. (Original) The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects the other end of said output side via wiring and the other end of said input side via wiring.

6. (Original) The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects the other end of said input side via wiring and a fixed voltage source.

7. (Original) The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects an output of a circuit other than said clock buffers and the other end of said input side via wiring.

8. (Currently Amended) The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects an output of a circuit other than said plurality of clock buffers and the other end of said output side via wiring.

9. (Currently Amended) The master slice semiconductor integrated circuit according to ~~claims~~ claim 4, further comprising a wiring which has a dummy load capacity equivalent to a load capacity connected to said input side via wiring, and is formed of said upper wiring layer and connected to the other end of said output side via wiring.

10. (Cancelled)

11. (New) A semiconductor device comprising:

a semiconductor substrate;

a first wiring layer above said semiconductor substrate, said first wiring layer being formed as a customized wiring layer such that a pattern of said first wiring layer is determined based on customer specifications;

a second wiring layer between said semiconductor substrate and said first wiring layer, said second wiring layer being formed as a fixed wiring layer such that a pattern of said second wiring layer is determined independently of the customer specifications;

a first clock output circuit formed in said semiconductor substrate and outputting a first clock signal through a first clock output wiring, said first clock output wiring being formed as said second wiring layer;

a first clock input circuit formed in said semiconductor substrate and receiving the first clock signal through a first clock input wiring, said first clock input wiring being formed as said second wiring layer; and

a first connecting wiring formed as said first wiring layer to make an electrical connection path between said first clock output wiring and said first clock input wiring.

12. (New) The device as claimed in claim 11, wherein each of said first clock output wiring and said first clock input wiring is embedded into an insulating film that covers said semiconductor substrate, said first connecting wiring being formed over said insulating film and connected to said first clock output wiring through a first via and to said first clock input wiring through a second via.

13. (New) The device as claimed in claim 11, further comprising:

a second clock input circuit formed in said semiconductor substrate and receiving the first clock signal through a second clock input wiring, said second clock input wiring being formed as said second wiring layer; and

a second connecting wiring formed as said first wiring layer to make an electrical connection path between said first clock output wiring and said second clock input wiring.

14. (New) A semiconductor device having a multilevel wiring structure including a lower-level wiring layer, an upper-level wiring layer and an insulating film intervening between said lower-level and upper-level wiring layers, said device comprising:

a first wiring formed as said lower-level wiring layer to convey a first clock signal;

a first via formed in said insulating film in contact with a part of said first wiring;

a second wiring formed as said lower-level wiring layer to convey a second clock signal;

a second via formed in said insulating film in contact with a part of said second wiring;

a third wiring formed as said lower-level wiring layer;

a third via formed in said insulating film in contact with a part of said third wiring;

a fourth wiring formed as said lower-level wiring layer;

a fourth via formed in said insulating film in contact with a part of said fourth wiring; and

a fifth wiring formed as said upper-level wiring layer in contact with each of said first via and said second via to thereby allow said first clock signal to be transferred to said second wiring;

said fourth via being supplied to one of a power potential and a third clock signal and being free from contact with said third via.

15. (New) The device as claimed in claim 14, further comprising a circuit, said third via being connected to said circuit to supply said second clock to said circuit.

16. (New) The device as claimed in claim 14, wherein said upper-level wiring layer is formed as a customized wiring layer such that a pattern of said upper-level wiring layer is determined based on customer specifications, and said lower-level wiring layer being formed as a fixed wiring layer such that a pattern of said lower-level wiring layer is determined independently of the customer specifications.

17. (New) The device as claimed in claim 14, wherein said first via is formed close to said third via and said second via is formed close to said fourth via.

18. (New) The device as claimed in claim 11, further comprising:

a second clock output circuit formed in said semiconductor substrate and outputting a second clock signal through a second clock output wiring, said second clock output wiring being formed as said second wiring layer;

a second input circuit formed in said semiconductor substrate and having a second clock input wiring, said first clock input wiring being formed as said second wiring layer;

a first via wiring formed in contact with a part of said second clock output wiring; and

a second via wiring formed in contact with a part of said second clock input wiring, said second via wiring being formed adjacently to said first via wiring with an electrical isolation therefrom.

19. (New) The device as claimed in claim 18, further comprising a second connecting wiring formed as said first wiring layer to make an electrical connection path between said first and second via wirings.